METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and a method for manufacturing the same and, more particularly, to an improvement in an element isolation technique of a metal oxide semiconductor large scale integrated circuit (MOSLSI) together with an improvement in a diffusion wiring layer and stabilization of a substrate potential.

Selective oxidation is generally adopted to isolate semiconductor elements from each other in the process for manufacturing a semiconductor device, especially, a MOSLSI. The selective oxidation will be described with reference to an n-channel MOSLSI.

As shown in FIG. **1A**, an SiO_2 film **2** is grown on a p-type silicon substrate **1** which has a crystal plane of (**100**). An Si_3N_4 film **3** is then deposited on the SiO_2 film **2**. A photoresist pattern **4** which corresponds to a prospective element formation region is formed by photoetching. Using the photoresist pattern **4** as a mask, part of the Si_3N_4 film **3** which does not correspond to the prospective element formation region is etched to form an Si_3N_4 pattern **3'**. Thereafter, boron is ion-implanted to form a p^+-type region **5** as a channel stopper in the field region (FIG. **1B**). After the photoresist pattern **4** is removed, a thick field oxide film **6** is selectively grown by wet oxidation using the Si_3N_4 pattern **3'** (FIG. **1C**) as a mask. The Si_3N_4 pattern **3'** and the SiO_2 film **2** are etched, and an element formation region **7** which is isolated by the field oxide film **6** is formed (FIG. **1D**). As shown in FIG. **1E**, a gate electrode **9** which comprises polycrystalline silicon is formed in the element formation region **7** through a gate oxide film **8**. Arsenic is ion-implanted in the element formation region **7** and is thermally diffused to form n^+-type regions **10** and **11** which are respectively defined as the source and drain. A CVD-SiO_2 film **12** which functions as an insulating interlayer is deposited. Contact holes **13** which correspond to the n^+-type regions **10** and **11** and the gate electrode **9** are formed in the CVD-SiO_2 film **12**. Aluminum wirings **14** are deposited in the contact holes **13** to prepare an n-channel MOSLSI (FIG. **1F**).

However, the various drawbacks are presented by the above-mentioned conventional thermal oxidation method for manufacturing the MOSLSI.

FIG. **2** is a detailed sectional view showing a structure when the field oxide film **6** is formed using the Si_3N_4 pattern **3'** as a mask, shown in FIG. **1C**. Generally, in the selective oxidation method, it is known that the field oxide film **6** grows to extend under the Si_3N_4 pattern **3'** (region F in FIG. **2**). Since an oxidant is diffused through the thin SiO_2 film **2** under the Si_3N_4 pattern **3'** during field oxidation, the field oxide film **6** has a portion D which is a bird's beak and a portion E which is a thick portion along the transverse direction of the field oxide film **6**. The length of region F is about 1 μm when the field oxide film **6** of 1 μm thickness is grown under the condition that the Si_3N_4 pattern **3'** and the SiO_2 film **2** have the thickness of 1,000 Å . A width C of the field region cannot be less than 4 μm since the length of the region F is 1 μm when a distance A between the Si_3N_4 patterns **3'** is 2 μm. As a result, a highly integrated LSI cannot be obtained. In order to eliminate the above drawback, a method has been recently proposed wherein the thickness of the Si_3N_4 pattern **3'** is increased and the thickness of the underlying SiO_2 film **2** is decreased to prevent the bird's beak (portion D). Alternatively, another method is proposed wherein the thickness of the field oxide film **6** is decreased to prevent formation of the region F. However, in the former method, the mechanical stress at the end of the field region is increased, resulting in the defective LSI. In the latter method, the field inverted voltage is decreased. Thus, high integration by the selective oxidation method is limited.

When boron is ion-implated to form a channel stopper, boron is transversely diffused during the field oxidation. Part of the element formation region **7** becomes the p^+-type region **5** as shown in FIG. **3A** due to redistribution of boron previously ion-implanted for the channel stopper in the transverse direction during field oxidation. The width of the effective element region is decreased from a width G to a width H. As a result, a current flowing through the transistor is decreased, and the threshold voltage is increased, resulting in the narrow channel effect. This effect is a significant problem when the semiconductor element is micronized. Further, since the p^+-type region **5** extends transversely, the p-n junction between the n^+-type region **11** (**10**) and the p^+-type region **5** is widened as shown in FIG. **3B**. The stray capacitance between the substrate **1** and the n^+-type regions **10** and **11** is increased. The stray capacitance cannot be neglected when the semiconductor element is micronized.

As described above, various problems are presented in manufacture of an LSI of a high packing density when the selective oxidation method is used. Further, the problems are described with reference to FIGS. **4** to **6**.

It is generally difficult to cross an n^+-type wiring layer **10'** and a polycrystalline silicon electrode **9'** on the field oxide film **6** (FIG. **4**). In order to cross the wiring layer **10'** and the electrode **9'**, the n^+-type layer **10''** must be formed under the field oxide film **6**. For this purpose, an impurity such as phosphorus or arsenic must be doped prior to field oxidation. In this case, since the concentration of the impurity is generally high, the n-type doped impurity is out-diffused at the initial period of field oxidation, so that the p-type region on the surface of the substrate may often be changed to an n-type region. When an n-type impurity is diffused in a gate region **1'**, the threshold voltage of the transistor is decreased. Further, according to the above method, when the n^+-type region is formed under the field oxide film **6**, margin **M1** between the n^+-type layers **10** and **10''** and margin **M2** between the n^+-type layers **10'''** and **10'** must be formed to isolate the n^+-type layers **10**, **10'** and **10'''**. Therefore, the field width becomes as great as **M1**+**M**+**M2**, and a highly integrated circuit cannot be provided.

Further, according to the conventional selective oxidation method, the following problems are also presented which will be described with reference to FIG. **7**.

In order to package an LSI pellet, a substrate **1** is mounted on a bed **15** of the package. When the LSI is operated, the potentials of element regions 16_1 to 16_3 for the source, drain and so on fluctuate in accordance with the operation state. In this case, a current flows through the substrate **1** in accordance with changes in the potentials of the element regions 16_1 to 16_3. For example, with respect to the element region 16_1, the current flows through a path of the element region 16_1, a resis-